

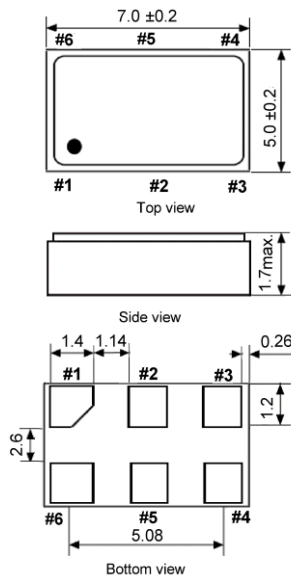


LVDS Clock Oscillator SMD-version

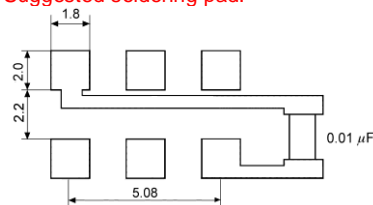
+1.8 / +2.5 / +3.3 V

part no.	12.xxxxx
model	KXO-V65
frequency range	10.0 ~ 800.0 MHz
frequency stability incl. temperature stability, input voltage and load stability, aging	±20, ±25, ±50 ppm over -20°C ~ +70°C / -40°C ~ +85°C (referred to +25°C) ±50, ±100 ppm over -55°C ~ +125°C (referred to +25°C)
output load	100 Ohm & 5 pF LVDS
operating temperature	standard -20° ~ +70°C available -40° ~ +85°C (=KXO-V65T), -55° ~ +125°C (=KXO-V65F)
storage temperature	-55° ~ +125°C
supply voltage	+1.8 V DC ±5 %, +2.5 V DC ±5 % or +3.3 V DC ±5 %
output voltage level	V _{OL} : 0.9 V min. / V _{OH} : 1.6 V max.
supply current max.	35 mA
start up time max.	10 ms
symmetry	45 % / 55 % at ½ V _{DD} level
rise time (Tr)/ fall time (Tf) max.	600 ps (Output level 20 % ~ 80 % of waveform)
disable delay/enable delay time max.	200 ns/4 ms
enable/disable (Pin 1) input voltage	30 % V _{DD} max.: output disable / 70 % V _{DD} min.: output enable
LVDS offset output voltage	1.125 V ~ 1.375 V, 1.250V typ.
tristate function	yes
phase jitter (12 kHz ~ 20 MHz)	RMS: 10.0 ~ 212,5 MHz 1 ps max. < 800,0 MHz 1.5 ps max.
typical phase noise	-70 dBc/Hz at 10 Hz -105 dBc/Hz at 100 Hz -130 dBc/Hz at 1 kHz -145 dBc/Hz at 10 kHz -145 dBc/Hz at 100 kHz -145 dBc/Hz at 1 MHz
contents of reel	1000 pcs.

Dimensions (mm):

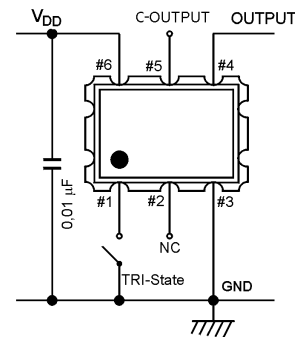


Suggested soldering pad:

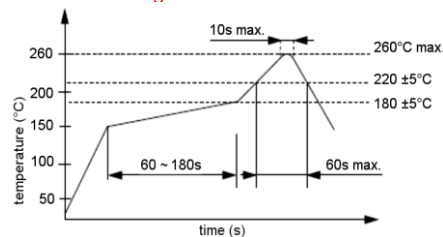


PIN	Connection
1	Tri-state or NC
2	NC
3	GND
4	Output
5	C-Output
6	V _{DD}

Test circuit:



Reflow soldering condition:



Tape specification:

