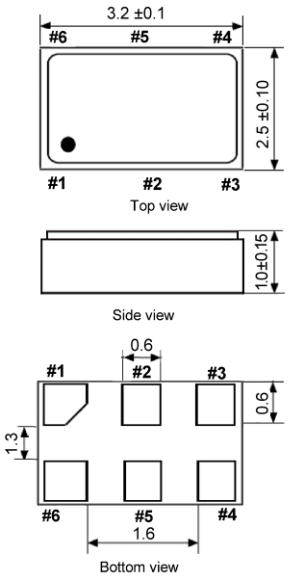
RoHS 2015/863/EU REACH compliant Conflict minerals free

GEYER quartz technology

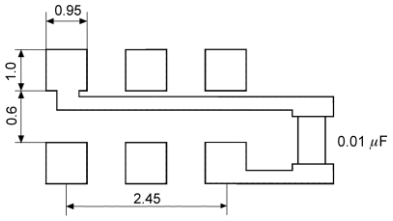
LVDS Clock Oscillator SMD-version +1.8 / +2.5 / +3.3 V

part no.	12.xxxxx
model	KXO-V64
frequency range	10.0 ~ 212.5 MHz
frequency stability incl. temperature stability, input voltage and load stability, aging.	±20, ±25, ±50 ppm over -20°C ~ +70°C / -40°C ~ +85°C (referred to +25°C) ±50, ±100 ppm over -55°C ~ +125°C (referred to +25°C)
output load	100 Ohm & 5 pF LVDS
operating temperature	standard -20° ~ +70°C available -40° ~ +85°C (=KXO-V64T), -55° ~ +125°C (=KXO-V64F)
storage temperature	-55° ~ +125°C
supply voltage	+1.8 V DC ±5 %, +2.5 V DC ±5 % or +3.3 V DC ±5 %
output voltage level	V_{OL}: 0.9 V min. / V_{OH}: 1.6 V max.
supply current max.	35 mA
start up time max.	10 ms
symmetry	45 % / 55 % at ½ V_{DD} level
rise time (Tr)/ fall time (Tf) max.	600 ps (Output level 20 % ~ 80 % of waveform)
disable delay/enable delay time max.	200 ns/4 ms
enable/disable (Pin 1) input voltage	30 % V_{DD} max.: output disable / 70 % V_{DD} min.: output enable
LVDS offset output voltage	1.125 V ~ 1.375 V, 1.250V typ.
tristate function	yes
phase jitter (12 kHz ~ 20 MHz) max.	RMS: 1 ps
phase noise typ.	-60 dBc/Hz at 10 Hz -90 dBc/Hz at 100 Hz -105 dBc/Hz at 1 kHz -115 dBc/Hz at 10 kHz -120 dBc/Hz at 100 kHz -130 dBc/Hz at 1 MHz
contents of reel	1000 pcs.

Dimensions (mm):



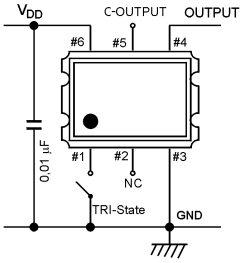
Suggested soldering pad:



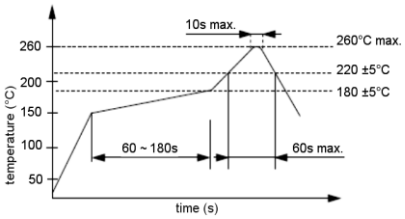
Note:
A capacitor of value 0,01µF and 10µF between V_{DD} and GND is recommended.

PIN	Connection
1	Tri-state or NC
2	NC
3	GND
4	Output
5	C-Output
6	V_{DD}

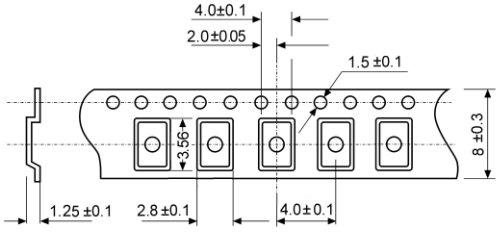
Test circuit:



Reflow soldering condition:



Tape specification:



reel diameter 178 mm

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