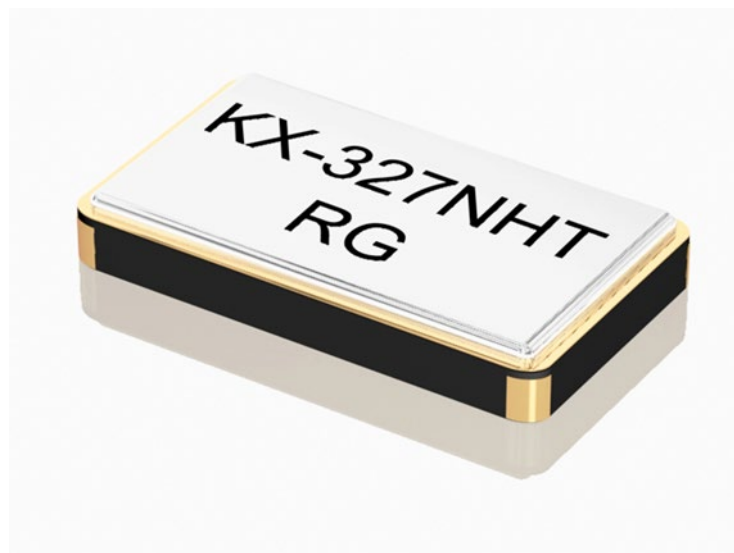# 32kHz Design
for
Low Power Applications

Reducing Power Consumption for 32kHz
Quartz Crystal Oscillator Circuit

Abstract

The intent of this investigation is to show the advantages of 32kHz crystals with reduced C_L and lower ESR over conventional 32kHz crystals with regard to power consumption, oscillation allowance, starting time and drive level.

The following draft confirms the advantage of the use of Geyer Electronic KX-327NHT with Load Capacitance of 7pF instead of 12,5pF.

Part number 12.87153	7pF	+/-20ppm	≤ 80k Ohm, 50k Ohm typ.
Part number 12.87148	7pF	+/-20ppm	≤ 50k Ohm, 35k Ohm typ.

- Considerably reduced Power Consumption
- Improved Start up Performance
- Faster Start up time
- Stable operation for lower drive level

## 1. Reducing Power Consumption in CMOS Oscillator Circuit

Current consumption of the crystal oscillator circuit depend on power supply voltage (V_{DD}), frequency, load capacitance, and R_1 of the quartz crystal.
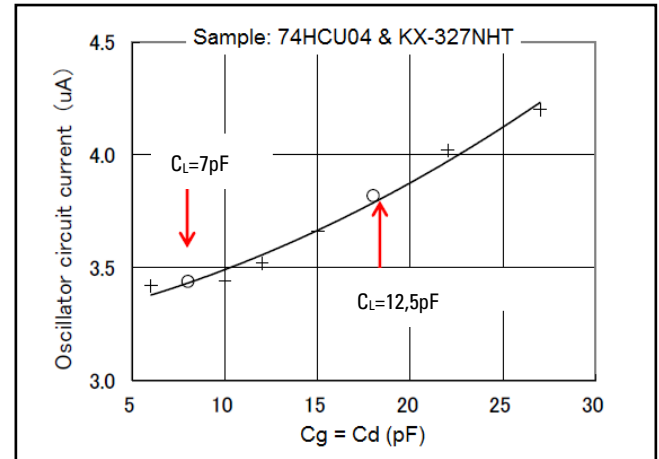
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* Current consumption in the oscillator circuit
    1. Charge and discharge current of C_L »   Low C_L
    2. Flow-through current   »   Low R_1

* Low-C_L and Low-R_1 of the quartz crystal realizes reduction of power
  consumption in the oscillator circuit

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2. Relationship for C_L and Power Consumption in the Oscillator Circuit
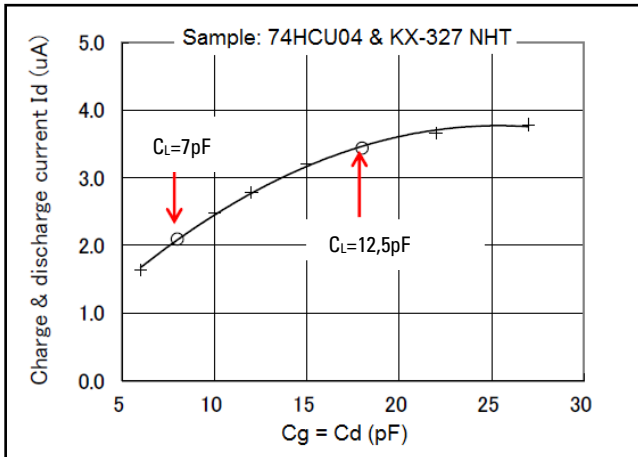

Charge and Discharge Current
ID (Calculation)

Oscillator circuit current
(Actual measurement)

$$Id = \frac{Vd}{1/(2\pi f)C_d} = (2\pi f)VdC_d$$

* Charge and discharge current for C_L=7pF is 40% lower than for of 12,5pF.

* Actual measurement includes the flow-through current of the oscillation inverter.
  Therefore, when the flow-through current is controlled, the calculated values
  Approximate the actual reduction of the current consumption.

[3]

3. Relationship of Negative Resistance (Oscillation Allowance) and C_L
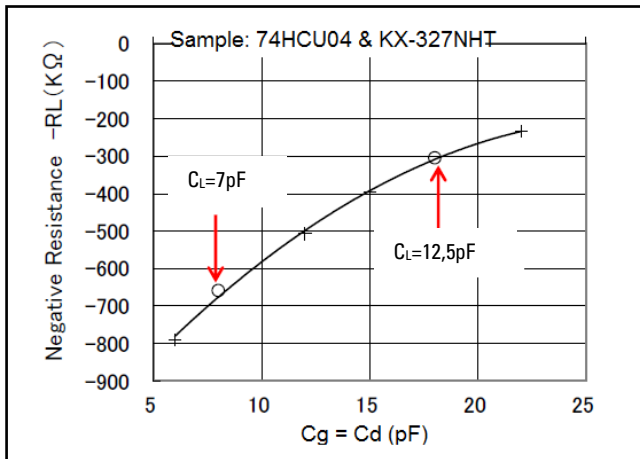
Negative Resistance $-R_L$ (KΩ)
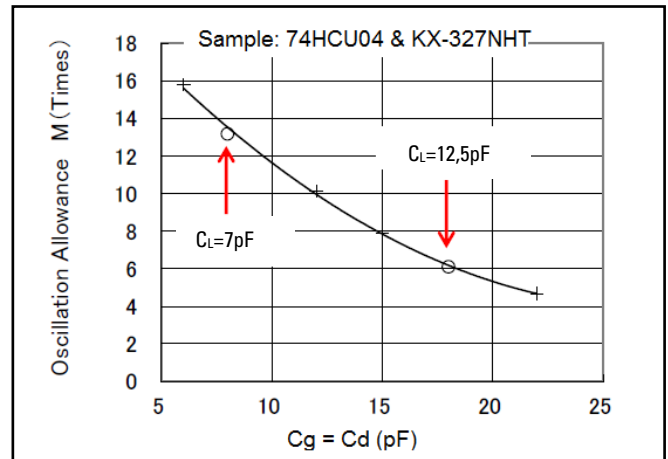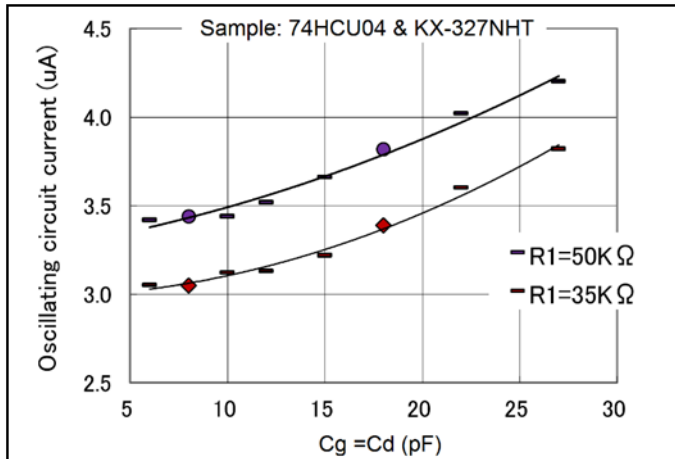

Oscillation Allowance M (Times)

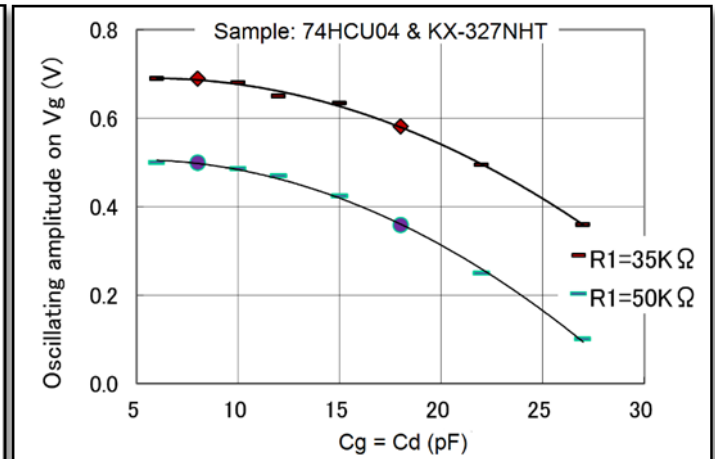$$-R_L = \frac{-g_m}{(2\pi f)^2 C_g C_d}$$

Reduction of gm and Vdd lowers the IC`s power consumption, which reduces the oscillation allowance.
The Crystal`s low $- C_L$ offsets the reduction of oscillation allowance.

4. Relationship for Oscillator circuit current and R_1

Oscillator circuit current
(Actual measurement)

Oscillator amplitude on C_g (V)

* The current consumption of an oscillator circuit using 74HCU04 can decrease by
  Approximately 10% based on the quartz crystal motional resistance R_1.

* Quartz crystal motional resistance R_1 will be higher, the oscillator amplitude on C_g will
  be lower, and the flow-through current of oscillator will be higher.

5. Another Advantage of Low-C_L (Oscillation Rising Time)

Low CL makes a higher negative resistance.
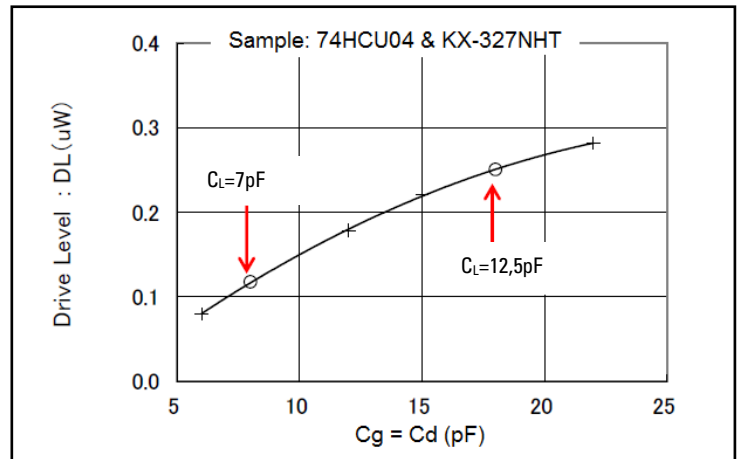The oscillator rising time will be shorter
if the C_L is lower.
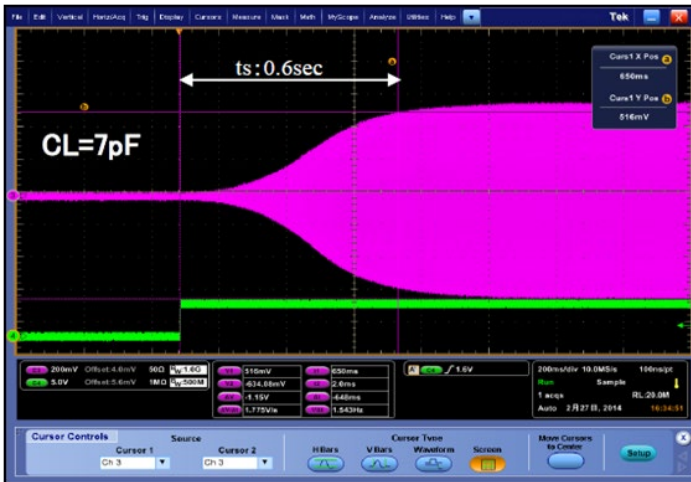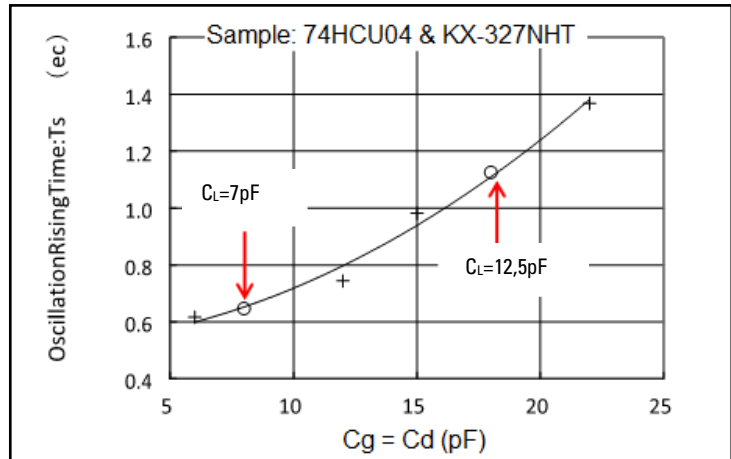
6. Another Advantage of Low-CL (Drive Level)

$$D_L = I^2 \times R_e$$

$$I = V_g / (1/\omega C)$$
$$R_e = R_1 \times (1 + C_o/C_L)^2$$

Lower C_L reduces the quartz crystal excitation current and reduced the drive level. Excessive drive level makes the characteristics of the tuning fork quartz crystal unstable.

7. Precision vs. Power Consumption

While a crystal with a low load capacitance of $C_L = 7pF$ provides a design with low power consumption, a crystal with a higher load capacitance of $C_L = 12,5pF$ is more advantageous for applications requiring higher precision.

As you can see from the diagram, the slope at $C_L = 7pF$ is steeper than that at $C_L = 12,5pF$. This means that circuit tolerances have stronger influence on a 7pF-crystal than on a 12,5pF-crystal.

KX-327NHT - 7pF

KX-327NHT – 12,5pF
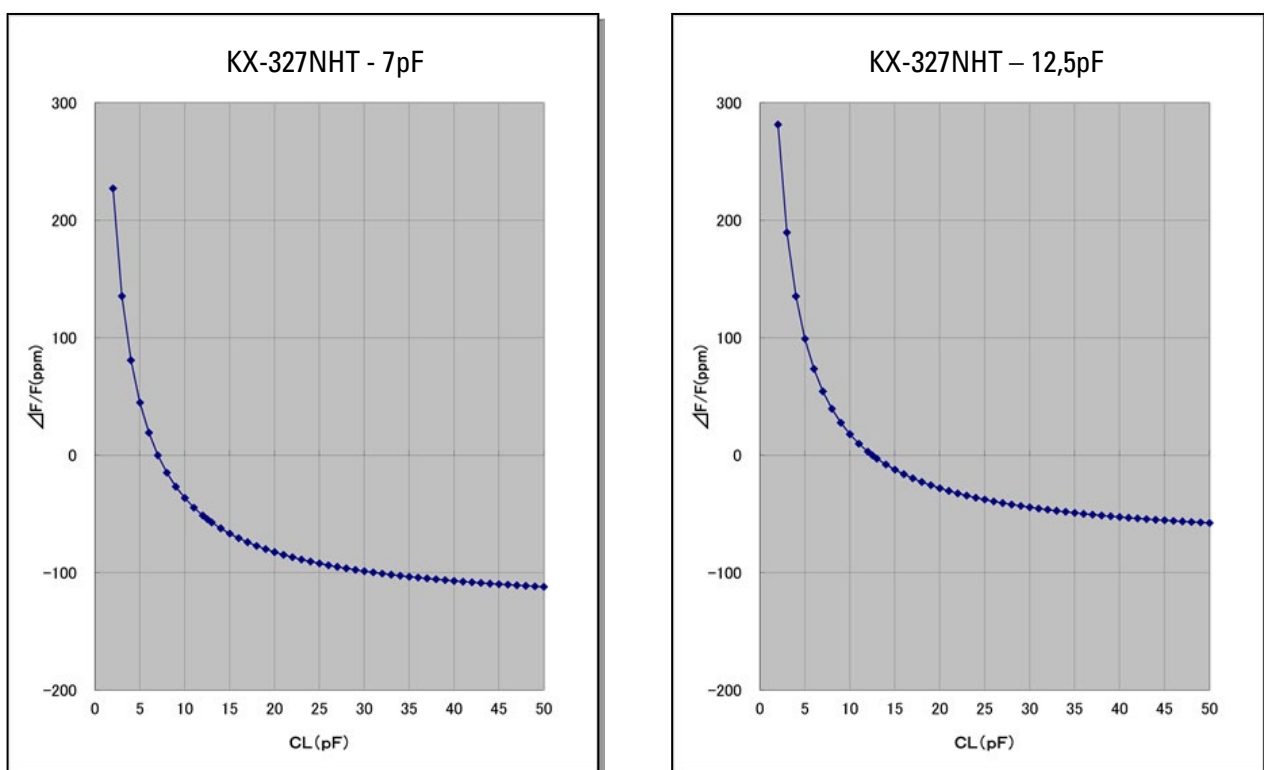
Therefore it is necessary to balance power consumption with precision.

Annex: Circuit Matching Investigation

Result of Matching Investigation

This is an example of our matching investigation for customers.
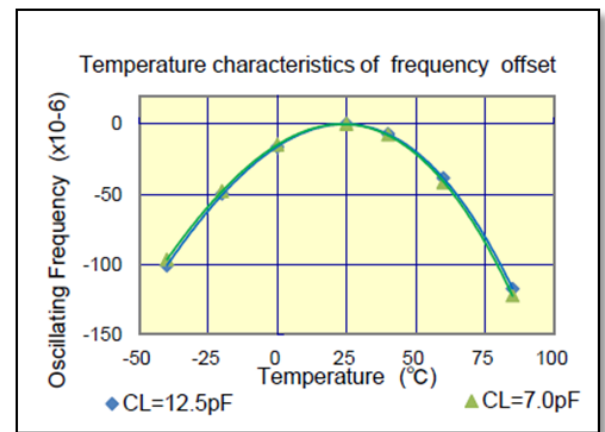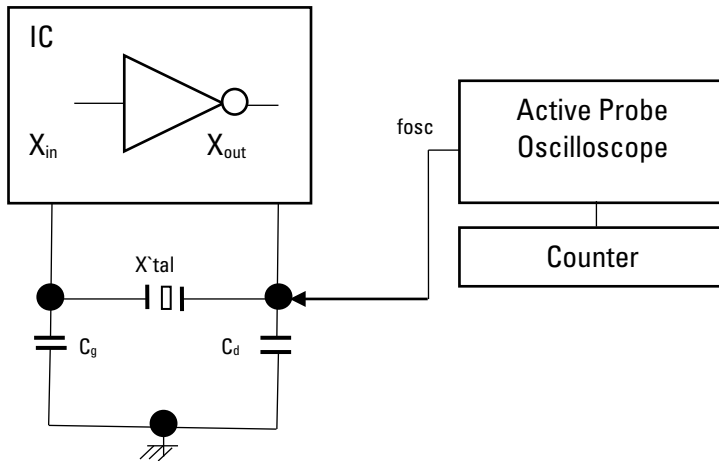
Our Crystal: KX-327NHT

Table 1. Constants

	A	B		
Key specifications	C_L 12,5pF	C_L 7pF	Unit	Remarks
V_{DD}: V	3,3	3,3		
Capacitance at Input: C_g	20	6	pF	Optimal capacitance in response to C_L
Capacitance at Output: C_d	20	6	pF	

Table 2. Characteristic data

Item	C_L 12,5pF	C_L 7pF	Unit	Remarks
Matching accurancy: f/F$_o$	2,50	1,19	$\times 10^{-6}$	Frequency offset at specified V_{DD}
Voltage Fluctuation: +/-df/V	-	0,00	$\times 10^{-6}$	V_{DD} +/-10% (Standard operating voltage range)
Drive Level: D_L	0,01	0,01	µW	$D_L = I \times 2 R_e < 1 \times 10^{-6} W$, $R_e = R_1 (1 + C_0/ C_L)2$
Negative Resistance: I −R_L I	-665	-1063	kOhm	**5 times larger than R$_1$MAX Judgemental standard of oscillation stability**
Oscillation Allowance: M	9,5	15,2	Times	
Oscillation Starting Voltage	-	1,43	V	
Oscillation Stopping Voltage	-	1,36	V	